WHAT IS CLAIMED IS:

1. A method of fabricating an array substrate for an active matrix type liquid crystal display (LCD) device, the method comprising:

a) forming a plurality of parallel, spaced apart gate lines, each gate line having a gate pad on an end, on a substrate by depositing a first metal layer on the substrate and then patterning the first metal layer using a first mask;

b) forming a gate insulating layer, a semiconductor layer, an ohmic contact layer, and a second metal layer by sequentially depositing a first insulating material, a semiconductor material, a doped semiconductor layer, and a metallic material on the substrate;

c) forming a plurality of data lines having data pads, a plurality of source electrodes, and a plurality of drain electrodes by patterning the second metal layer using a second mask, wherein the data lines cross the gate lines, wherein said source electrodes extended from the data lines adjacent the crossings of the gate lines and the data lines, and wherein the drain electrodes are spaced apart from the source electrodes;

d) forming a plurality of channel regions by etching portions of the ohmic contact layer using the patterned second metal layer as a mask, wherein the channel regions are defined on the semiconductor layer between source and the drain electrodes;

e) depositing a second insulating layer on the structure that results from step d);

f) patterning the second insulating layer to form a passivation layer having a plurality of data pad contact holes that expose data pads and a plurality of drain contact holes that expose drain electrodes, wherein the passivation layer covers the patterned second metal layer and a peripheral portion of the gate lines; and

g) forming a plurality of pixel electrodes, data pad electrodes, and gate pad electrodes by depositing a transparent conductive layer on the passivation layer, and then patterning the transparent conductive layer using a fourth mask, wherein portions of the pixel electrodes overlap peripheral portions of gate lines, wherein the pixel electrodes electrically connect with drain electrodes via the drain contact holes, wherein the data pad electrodes electrically connected with data pads via the data pad contact holes, and wherein the gate pads electrically connect with the gate pads via the gate pad contact holes.

2. The method according to claim 1, further including the step of forming short-preventing regions comprised of the second insulating layer, the semiconductor layer, the ohmic contact layer, the second metal layer, and the first insulating layer.

3. The method according to claim 1, wherein the depositing of a transparent conductive layer deposits a material that includes indium.

4. The method according to claim 1, wherein the depositing of a semiconductor layer deposits an amorphous silicon.

5. A method of fabricating an array substrate for an active matrix type liquid crystal display (LCD) device, said method comprising:

a) depositing a first conducting material on a substrate;

b) using a first mask to form a gate line having a gate pad at one end on the substrate;

c) sequentially depositing a first insulating layer, a semiconductor layer, an ohmic contact layer, and a second conducting material over the structure resulting from said step b);

d) using a second mask to pattern said second conducting material to form a data line that crosses said gate line, a source electrode adjacent said crossing, and a drain electrode adjacent said crossing point;

e) defining a channel region between said source and drain electrodes by etching said ohmic contact layer using said source and drain electrodes as a mask;

f) forming a passivation layer by depositing a second insulating layer over the structure resulting from said step e);

g) using a third mask to form a drain contact hole that exposes the drain electrode;

h) depositing a transparent conductive material over the structure resulting from step g); and

i) using a fourth mask to form a pixel electrode such that said pixel electrode electrically connects to said drain electrode.

6. The method of claim 5, wherein said first conducting material is selected from a group comprising molybdenum (Mo), chromium (Cr), and aluminum-neodymium-molybdenum alloys.

7. The method of claim 5, wherein said second conducting material is selected from a group comprising molybdenum (Mo), chromium (Cr), and aluminum-neodymium-molybdenum alloys.

8. The method of claim 5, wherein in step d), said source electrode is formed by extending a portion of said data line in a direction of said gate line.

9. The method of claim 5, wherein said drain electrode extends into a rectangular region that is defined by gate lines and data lines.

10. The method of claim 5, wherein said transparent conductive material includes indium.

11. The method of claim 5, wherein said pixel electrode extends over a portion of said gate line so as to form a storage capacitor from said portion of said gate line, said extended portion of said pixel electrode, and said gate insulating layer.

12. The method of claim 11, further including the forming of a short-preventing part between an edge of said gate line and said pixel electrode.

13. The method of claim 12, wherein said short-preventing part includes portions of said first insulating layer, said semiconductor layer, said ohmic contact layer, said second conducting material, and said passivation layer.

14. The method of claim 12, wherein said short-preventing part includes portions of said first insulating layer, said semiconductor layer, and said passivation layer.

15. The method of claim 12, wherein a plurality of short-preventing parts are formed.

16. The method of claim 15, wherein the plurality of short-preventing parts form step portion at said gate line.

17. The method of claim 15, wherein the short-preventing parts are scattered on said gate line.

18. The method of claim 12, wherein the short-preventing part covers the width of the overlapped portion of said gate line.

19. An array substrate for an active matrix type liquid crystal display (LCD) device, comprising:

a substrate;

a gate line on said substrate, wherein said gate line includes a gate pad;

a first insulating layer on said gate line and said substrate;

a semiconductor layer on said first insulating layer and over a portion of said gate line;

a data line over said first insulating layer and that crosses said gate line, said data line including a protruding portion that projects in a direction of said semiconductor layer and that forms a source electrode, wherein said data line further includes a data pad;

a drain electrode space apart from said source electrode and extending into a rectangular region partially defined by said gate and data lines;

a passivation layer on said drain electrode, said passivation layer having a drain contact hole that exposes said drain electrode; and

a pixel electrode formed over the passivation layer, said pixel electrode electrically connecting to said drain electrode via said drain contact hole, wherein said pixel electrode extends over a portion of said gate line so as to form a storage capacitor comprised of said pixel electrode, said gate line, and said first insulating layer, wherein said storage capacitor further includes a short-preventing part disposed between said pixel electrode and said gate line.

20. The array substrate of claim 19, wherein said short-preventing part includes said semiconductor layer and said passivation layer.

21. The array substrate of claim 20, wherein said short-preventing part further includes an ohmic contact layer, and a conducting material between said semiconductor layer and said passivation layer.